IN THE CLAIMS:

Please amend claim 1 and add claims 8-13 as follows:

Claim 1 (Currently Amended): A semiconductor device comprising:

~~an~~ a first interconnect layer arranged above a surface of a substrate on which a functional semiconductor region is formed;

an inter layer dielectric covering a surface of said first interconnect layer~~, and~~;

a silicon nitride film formed so as to cover a whole surface of said inter layer dielectric;

a metal interconnect layer ~~as an uppermost metal layer formed as an upper layer of~~ covering said silicon nitride film, said metal interconnect layer being consisted of gold material; and

a planarized dielectric formed on said metal interconnect layer.

Claim 2 (Original): A semiconductor device according to claim 1, wherein said planarized dielectric is consisted of polyimide.

Claim 3 (Original): A semiconductor device according to claim 2, wherein said silicon nitride film is formed by high-density plasma CVD method.

Claim 4 (Original): A semiconductor device according to claim 1, wherein polyimide resin layer is removed at a part of region of said metal interconnect layer and bonding wire is connected to said region in said metal interconnect layer.

Claims 5-7 (Withdrawn).

Claim 8 (New): A semiconductor device comprising:

a first interconnect layer covering a first portion of a surface of a functional semiconductor region;

an inter layer dielectric covering a second portion of the surface of the functional semiconductor region and a portion of a surface of said first interconnect layer, thereby forming a contacting hole on the surface of the first interconnect layer;

a silicon nitride film covering an entire surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region;

a metal interconnect layer consisting of gold material covering the barrier layer region, thereby forming a metal interconnect region; and

a planarized dielectric covering the metal interconnect layer and the silicon nitride surface around the metal interconnect region.

Claim 9 (New): The semiconductor device of claim 8, wherein the barrier layer consists of titanium.

Claim 10 (New): The semiconductor device of claim 9, wherein the first interconnect layer consists of aluminum.

Claim 11 (New): The semiconductor device of claim 8, wherein the first interconnect layer consists of aluminum.

Claim 12 (New): The semiconductor device of claim 8, wherein the inter layer dielectric consists of USG film.

Claim 13 (New): The semiconductor device of claim 8, wherein the functional semiconductor region further comprises a polysilicon gate isolated from the first interconnect layer by a second dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer.